Jordan University of Science and Technology
Computer Engineering Department
CPE 552-Computer Design-HW2
Dr. Lo'ai Tawalbeh-Spring 2009

Problem 1.

Consider the block diagram for an adder/subtractor shown in Figure 1. The unit is able to add and subtract numbers represented in two's complement. For the following pairs of 8-bit vectors X and Y representing integers in the two's complement system, obtain the 8-bit vectors Z and D, representing $Z = X + Y$, and $D = X - Y$, respectively. For that, prepare a table showing the values of the control signal Ky, carry-in bit c_0, and the bit-vectors at the output of the complementer and at the output of the adder as well as the conditions for the output: *overflow* - ovf (recall that $ovf = c_7 \oplus c_8$, where c_7 and c_8 are the carry bits coming out of bit positions 6 and 7 respectively), *zero* (result equals zero), and *sign* (has a value 1 if the result is negative).

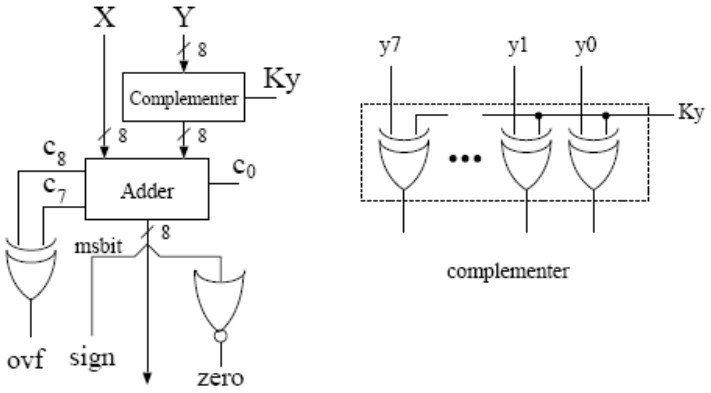

Figure 1: Adder/subtractor block diagram

X	Y
01010011	00100111
01010011	01000001
10101010	10100000
10110110	01100111

Problem 2.

This problem has two parts:

- Using **conditional signal assignment statements**, write and simulate the VHDL description of a 3-bit binary decoder. Test the model for all possible input combinations and print the decoder waveforms. Include an *enable* input in your design. When $enable = 0$, all decoder outputs are zeros.

- Using the 3-bit decoder as a component, implement a 6-bit decoder.

  There are two possible approaches: tree decoding or coincident decoding.

  - using tree decoding the outputs of the highest level 3-input decoder in the tree (root) are connected to the enable inputs of 8 different decoders in the second level of the tree. The decoders in the second level generate 64 signals altogether (outputs of a 6-bit decoder). This design requires 9 3-input decoders.
  - using coincident decoding the outputs of two decoders (one for each group of 3 bits) are combined by AND gates (one for each output of the 6-input decoder). The output that corresponds to input $(010011)_2 = (19)_{10}$ is obtained by the SE: $OA2$ and $OB3$, where $OA2$ is the output of decoder A, a decoder connected to the most significant bits of the input (010), and OBi is the output of decoder B, which is connected to the least significant input bits (011). A total of 64 2-input AND gates and two 3-input decoders are required in this case. Reference: *Introduction to Digital Systems, Ercegovac and Lang*, pages 246-250.

  Use one of these methods to obtain a 6-input decoder with *enable* input. Test the model for some possible input combinations and print the decoder waveforms.

Attach a printout of the simulation results in your homework.

Problem 3.

Write a VHDL code to describe an 8-input multiplexer using the **selected signal assignment statement**. Compile and simulate your description with a set of input vectors that represent a good test for the switching function that the multiplexer implements. Attach a copy of your VHDL code and the simulation results to your homework solution. Provide on the simulation printout any information that helps to convince that your simulation results are correct.